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13. ABSTRACT

As stated in our proposal, our research goal was to "derive architectures which preserve the VLSI implementation advantages of regular meshes while still obtaining sufficient increases in performance and/or decreases in size and cost." Our problem domain was signal and image processing applications which require either significant computational resources or which must be solved in real time. Our research has been successful in that we have derived a number of such architectures for important problem areas in image and signal processing. These architectures are outlined in more detail in the final report. We even successfully prototyped one of our architectures, the Arithmetic Cube, which involved both VLSI chip and PCB board design and fabrication. The Arithmetic Cube, directly solves both the discrete Fourier transform and cyclic convolution. In parallel with our architecture work, we also investigated algorithms which map efficiently onto the various derived architectures and which take advantage of their particular architectural aspects.

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SIGNAL PROCESSING ALGORITHMS FOR HETEROGENEOUS ARCHITECTURES

FINAL REPORT

MARY JANE IRWIN AND ROBERT MICHAEL OWENS

AUGUST 1, 1993

U. S. ARMY RESEARCH OFFICE

CONTRACT NUMBER: DAAL03-87-K-0118

THE PENNSYLVANIA STATE UNIVERSITY
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SIGNAL PROCESSING ALGORITHMS FOR HETEROGENEOUS ARCHITECTURES

1 JULY 1987 - 31 OCTOBER 1991

FINAL REPORT

1.A. STATEMENT OF THE PROBLEM STUDIED

As stated in our proposal, our research goal was to "derive architectures which preserve the VLSI implementation advantages of regular meshes while still obtaining sufficient increases in performance and/or decreases in size and cost." Our problem domain was signal and image processing applications which require either significant computational resources or which must be solved in real time. Our research has been successful in that we have derived a number of such architectures for important problem areas in image and signal processing. These architectures are outlined in more detail in the next section. We even successfully prototyped one of our architectures, the Arithmetic Cube, which involved both VLSI chip and PCB board design and fabrication. The Arithmetic Cube, directly solves both the discrete Fourier transform and cyclic convolution. In parallel with our architecture work, we also investigated algorithms which map efficiently onto the various derived architectures and which take advantage of their particular architectural aspects.

1.B. SUMMARY OF THE MOST IMPORTANT RESULTS

The results of the research supported by this three year ARO grant falls in two primary areas: architecture and algorithms, and in one secondary area: design tools. We will address the research results in each of these areas in turn.

In the architecture area we developed a number of new systolic VLSI architectures for computationally demanding applications. The first such systolic VLSI architecture can achieve real-time isolated word recognition for large dictionaries. The design is based on the dynamic time warping (DTW) algorithm, an exhaustive search technique which permits nonlinear pattern matching between an unknown utterance and a reference word. Our design differs from previous systolic DTW designs in that (1) all data is represented in signed-digit, base 4 format; (2) digits are passed between processing elements in a most significant digit first, digit serial fashion; and (3) the algorithms are pipelined at the digit level. Using most significant digit first data flow allows digit pipelining to succeed where conventional bit-serial pipelining has failed for the arithmetic operations required in the DTW algorithm. This allows a very high degree of concurrency and a high data rate to be maintained, while the pin out requirements are kept low. The VLSI DTW design presented is both flexible and modular. It is independent of the number of coefficients per frame and the precision of those coefficients. The design is also easily expandable in the number of frames per word and the warp factor used to achieve the nonlinear matching. Using our dynamic time warp processor design, real time word recognition of 100,000 word vocabulary is possible. Furthermore, because the processor is area efficient only a few VLSI chips would be needed.

Another of our new systolic VLSI architectures can be used to determine how well two two-dimensional images match. These space warp arrays are similar to the time warp array except that instead of matching in one temporal dimension (amplitude vs time), the space warper matches in two spatial dimensions (amplitude vs space x space). In this way the dynamic space warp VLSI array is the two-dimensional analog to the dynamic time warp array for one dimensional signals. Such arrays can be used to form the basis of an image recognition system. The design of the arrays is based on being able to expand and contract the two images with respect to one another so that a best matching is obtained. The one array, the image warp array, expands and contracts the two entire images with respect to one another so that a best matching can be obtained. The other array, the line warp array, finds, for each vertical or horizontal line in one image, the best match for that line in the second image. The distance between the two images is the sum of all the line distances for all the vertical and horizontal lines. An advantage of the line warp array is that it involves a three-dimensional wave front array versus the four-dimensional wave front array required for the image warp array. We show that an efficient and robust VLSI design is possible if local feature matching is used. For example it would be possible to build a space warper which could match (in the same sense that two word are matched by a time warper) thirty 1024 by 1024 pictures per second.

Yet another of our new systolic VLSI architectures, which we call the Arithmetic Cube, directly solves both the discrete Fourier transform and convolution based on the so-called small n algorithms. Most VLSI architectures proposed for computing these functions

use either a straightforward matrix times vector approach or use data shuffling to reduce the number of arithmetic operations. However, matrix times vector architectures compute many more operations than are necessary. While data shuffling architectures have VLSI implementation problems, in part, due to the inability of obtaining a bounded length or nearest neighbor interconnect structure in VLSI. The Arithmetic Cube computes no more multiplications than are necessary and has a regular bounded length, nearest neighbor interconnect structure. Using funds received from the National Science Foundation a full prototype of the Arithmetic Cube was constructed. This prototype is presently fully operational and is installed in a Sun-4 workstation.

Also in the architecture area we developed three new systolic, very fine grained architectures. To maintain their fine grainness most fine grain processors are relatively inflexible. Any attempt to increase flexibility increases processor complexity and, thereby, decreases grainness. The architecture we developed maintains both a high degree of flexibility and fine grainness. These micro grained architectures are especially suited for problems with a high degree of parallelism. In the first of these architectures each processor is an associative memory word. However, unlike other associative memory processors, ours uses a two-dimensional interconnect and a physically compact memory word structure. Arithmetic operations are based on the use of a redundant number system. These features provide an even higher level of performance. This is particularly true for certain two-dimensional problems. For example, we were able to show that an array which is capable of performing a 3x3 two-dimensional Laplacian over a 256x256 image in as little as 200 microseconds using as few as sixteen VLSI chips could be built.

The other two micro grained architectures were inspired by our interest in deriving architectures suitable for implementation by programmable logic devices (PLD's). Like PLD's the processors (cells) of our architectures consist of a few small RAM's and a local interconnect structure. Unlike PLD's, our architectures use a less general global interconnect structure. However, what we loose in generality, we make up for in speed especially for the problems of interest to us. These two architectures differ mostly in how the local function is computed. The one architecture uses RAM's just like some varieties of PLD's. The other uses muxes just like other varieties of PLD's. We have shown (via fabrication through MOSIS) that VLSI chip containing over 4096 processors can be built.

Another example of our work in the area of architectures for computationally demanding applications, is a simple memory array architecture we call the Access Constrained Memory Array Architecture (ACMAA). The architecture consists of a linear array of processors concurrently accessing rows or columns on an array of memory modules. This organization has a simple and regular structure and hence is very efficient for VLSI implementation. Parallel algorithms for various graph algorithms (bridge detection, transitive closure, shortest path), for image enhancement (contrast enhancement and edge detection), and for region(connected component) labeling have been developed which take advantage of the structure of the memory architecture.

We have also developed several architectures for signal processing problems which require designs with feedback paths. Such architectures are often limited in performance because of the time required to wait for the feedback data. In particular, we developed an architecture for IIR filters based on a new algorithm. We have also found that digit serial architec-

tures, with both high throughput and low system latency, can be used very effectively in designs with feedback paths. Such architectures can exploit digit pipelining - overlapping the input with the computation. Our work has concentrated on the design of various IIR filters based on digit serial components.

Finally, in the architecture area we have investigated a number of architectures which can perform matrix transpositions for two and higher dimensions. Efficient solutions to this problem would be of use in many signal processing architectures. Currently, we are examining two approaches. The first is a conceptual approach applicable to matrices of any dimension. In this approach, matrix elements are placed in equivalence classes under the operation of cyclic index shift. The transpose operation is effected by permuting elements within each equivalence class. We are studying methods for performing the permutations. The second approach is systolic in nature and is applicable to two dimensional matrices. Each cell connects to three neighbors to the left, three to the right. The cell consists of a three-by-three crossbar switch and some simple control for routing the inputs from the left to the output on the right. The routing algorithm is completely local in nature.

Next we outline our results in the algorithm area. Our algorithm work has, to some degree, paralleled our architecture work.

In the area of image recognition we have developed algorithms based on the concepts of local-distance diagrams, dynamic programming, and the minimum principle. The first algorithm (i.e., the dynamic space-warping algorithm (DSWA)) is used to find the minimum distance between two areas. The second algorithm (i.e., the dynamic line-warping algorithm (DLWA)) is used to find the minimum distance between a line and an area. For each of these image recognition algorithms, we need to consider both recognition rates and computational performance. We have shown experimentally that the DSWA has good recognition performance. However, more experiments need to be done to verify that the DLWA has satisfactory recognition rates. Intuitively, the DSWA can be implemented with a four-dimensional wavefront architecture and the DLWA can be implemented with a three-dimensional wavefront architecture.

We developed several new families of algorithms for the Arithmetic Cube II. As it stands the Arithmetic Cube II is "optimized" for computing the small n DFT and convolution algorithms for which n lies in a small range. Algorithms for which n is too large simply can not be computed. Algorithms for which n is too small under utilize the hardware on the Cube. To alleviate this situation, we have also shown how changing the dimensionality of a transform can be used to efficiently compute an arbitrary sized problem on an Arithmetic Cube of given size. For example we showed how either the discrete Fourier transform of n points or the cyclic convolution of two length n sequences can be performed on the Arithmetic Cube whose area is A in time $O(\frac{n}{\sqrt{A}}\log(\frac{n}{\sqrt{A}})+\sqrt{n})$. This time bound is within a $\log(\frac{n}{\sqrt{A}})$ factor of the lower bound of $\Omega(\frac{n}{\sqrt{A}}+\sqrt{n})$. Note that even if n and A differ by several orders of magnitude, this factor is small. Furthermore, even for a small Arithmetic Cube, our bound is no worse than performing the fast Fourier transform. We have also developed several new small n algorithms for the Cube which make better use of its architecture.

We developed a new algorithm for IIR filters. This algorithm obtains a high degree of parallelism, lower computational complexity than the block methods, and higher stability than the back substitution methods.

We have either modified existing algorithms or developed new algorithms for our micro grained and Access Constrained Memory Array Architectures. These algorithms include various graph algorithms (bridge detection, transitive closure, shortest path), image enhancement (contrast enhancement and edge detection) algorithms, and region (connected component) labeling algorithm. Also arithmetic algorithms for the elementary functions (addition, multiplication, division, trig, etc) have been developed which are especially suited for our micro grained architectures.

While our architecture and algorithm work was (and still is) the driving force of our research, we also have developed and/or acquired the necessary CAD tools to enable us to quickly prototype our architectures. In particular, we have developed the CAD tools which allow us to directly synthesis complete processors. Our processor synthesizer takes as input a hierarchical description of the computation to be performed and some hint as to how it is to be performed and outputs a detailed report on the hardware requirements for the specified computation, including the structure of each compute node, how they are connected, and the input and output sequences. Our module generation takes as input a hierarchical netlist description of a module and outputs a CMOS VLSI layout of the module.

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1.D. PARTICIPATING SCIENTIFIC PERSONNEL

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Robert Michael Owens, Associate Professor of Computer Science

Graduate Students

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Peng Zhang (supported Summer 1988) M.S., Computer Science, Summer 1989.

C-M Wu (supported Spring 1988 - Summer 1989) Ph.D., Computer Science, Fall 1989.

T-T Hwang (supported Fall 1989, Summer 1990), Ph.D., Computer Science, Fall 1990.

P-P Hou (supported Summer 1989 - Summer 1990) Ph.D., Computer Science, Spring 1991.

Gueesang Lee (supported Summer 1990), Ph.D., Computer Science, Summer 1991.

Soohong Kim (supported Summer 1990) Ph.D., Computer Science, August 1992.

Tom Kelliher (supported Summer 1988, Summer 1989, and Summer 1991) Ph.D., Computer Science, Spring 1993.

Mohan Vishwanath (supported Fall 1990 - Summer 1991), Ph.D., Computer Science, Spring 1993.

Kong-Yee Pun (supported Summer 1988), Ph.D. Candidate, Computer Science.

2. REPORT OF INVENTIONS

The following three invention disclosure were filed by the participating faculty in the fall of 1986.

PSU 86-751: An Area Efficient VLSI FIR Filter

PSU 86-752: The Arithmetic Cube

PSU 86-753: Digital Pipeline Dynamic Time Warp Processor

In November 1987, the University declined to elect title to the subject inventions and released them to the participating faculty. The Department of the Army subsequently offered no objection to the participating faculty seeking patent rights for the subject inventions. As of this date the participating faculty have not applied for patent rights. A copy of the relevant releases are attached.

DEPARTMENT OF THE ARMY
ARMY RESEARCH OFFICE
P.O. BOX 12211
RESEARCH TRIANGLE PARK, NC 27709-2211

REPLY TO ATTENTION OF

January 25, 1993

Procurement Office

Dr. Mary J. Irwin
The Pennsylvania State University
Eberly College of Science
Computer Science Department
333 Whitmore Laboratory
University Park, PA 16802

Subject: Invention under Contract #DAAG29-83-K-0126, "An Area Efficient VLSI FIR Filter (PSU 86-751), The Arithmetic Cube (PSU 86-752), Digital Pipelined Dynamic Time Warp Processor (PSU 86-753)"

Dear Dr. Irwin:

Pennsylvania State University has declined to elect title to the subject invention. Pennsylvania State University informed us, by letter dated, December 21, 1992, that you have expressed an interest in retaining certain rights to the invention to pursue a possible patent application.

This office offers no objection to the inventor seeking patent for the subject invention provided:

a. The Government receives a confirmatory license in accordance with the patent clause of the prime contract. A copy of such clause can be obtained from the prime contractor.

b. A copy of the patent application is provided to this office.

c. Sponsorship of the research effort is acknowledged in the patent application and resultant patent.

Please advise the undersigned if the conditions set forth in this letter are acceptable to you.

Sincerely,

Larry E. Travis

Larry E. Travis
Chief, Procurement Operations Branch

cc: Dr. Robert M. Owens

DEPARTMENT OF THE ARMY
UNITED STATES ARMY LABORATORY COMMAND
ARMY RESEARCH OFFICE
P.O. BOX 12211, RESEARCH TRIANGLE PARK, NC 27709-2211

November 12, 1987

REPLY TO ATTENTION OF:

Procurement Office P-20090-EL

Subject: ARO Contract No. DAAG29-83-K-0126
Invention Disclosures: PSU 86-751, 86-752 and 86-753

The Pennsylvania State University
Office of Sponsored Programs
ATTN: Mr. William D. Moir
Director
5 Old Main Building
University Park, Pennsylvania 16802

Gentlemen:

By your letter of September 11, 1987 you disclosed inventions under the subject contract with R . F. Owens and M. J. Irwin listed as inventors.

You indicated that the university will not file patent applications. However, you requested that the university be permitted to release title to the inventions to the inventors. We hereby give approval of this request.

In the event the inventors file, they are required to issue the Government a nonexclusive, nontransferable, irrevocable, paid-up license along with the patent application.

If they decide not to file patents, please notify this office immediately. We must receive notification prior to the end of any statutory period wherein valid protection can be obtained in the United States after a publication, or sale or public use.

If you have any questions regarding this matter, please contact me at telephone (919) 549-0641.

Sincerely,

Patsy S. Ashe

Patsy S. Ashe
Contracting Officer

Copy Furnished:

ONR

THE PENNSYLVANIA STATE UNIVERSITY

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November 19, 1987

Professor Robert M. Owens
College of Science
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308 Whitmore Laboratory
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Professor Mary Jane Irwin
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The Pennsylvania State University
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University Park, PA 16802

Re: "An Area Efficient VLSI FIR Filter,"
by R. M. Owens and M. J. Irwin
Our Ref: 86-751

Professors:

In response to your request dated July 14, 1987, having reviewed the various factual elements requisite to release, the University agrees to release to you the invention referenced above on the condition you agree:

1. Not to use the University or the University's name in the exploitation of such invention.

2. That the University may retain a license for University purposes.

3. That you will convey to the University or any sponsor such rights as are necessary to fulfill the obligations of the University to other parties, specifically, that you will comply with the federal government requirements set forth in the attached letter.

November 19, 1987

Professors R. M. Owens and M. J. Irwin
Re: "An Area Efficient VLSI FIR Filter"
Our Ref: 86-751

Please indicate your agreement and acceptance of this condition by adding your signatures and the dates thereof in the spaces provided below before returning this letter to me.

Yours truly,

Forrest J. Remick

FJR:RLH:mg
Attachment

AGREED TO AND ACCEPTED:

Mary Jane Irwin — Date: Dec. 2, 1987

Robert M. Owens — Date: Dec 2, 1987

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6. AUTHORS
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The view, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT

Simulation of hardware is a commonly used method for demonstrating that a circuit design will work for a restricted set of inputs. *Verification* is a method of proving a circuit design will work for all combinations of input values. Switch-level verification works directly from the circuit netlist.

The performance of existing switch-level verifiers has been improved through a combination of techniques. First, efficient methods of finding paths in the switch-graph are developed. Secondly, static analysis of the switch-graph is proposed to accelerate verification of sequential logic. Thirdly, cell replication is exploited in a safe way to make possible the verification of large hierarchical circuit design.

These ideas have been implemented in a program called V, which is part of the Penn State Design System. Experimental results are presented.

14. SUBJECT TERMS
Switch-level simulation, switch-level verification, switch-graphs, combinational and sequential verification, hierarchical verification

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4. TITLE AND SUBTITLE
C-Testability of Unilateral and Bilateral Sequential Arrays

5. FUNDING NUMBERS
DAAL03-87-K-0118

6. AUTHORS
S. Rawat and M.J. Irwin

7. PERFORMING ORGANIZATION NAME AND ADDRESS
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11. SUPPLEMENTARY NOTES
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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12b. DISTRIBUTION CODE

13. ABSTRACT

C-testability, sequential systolic arrays, design for test, LSSD test We study C-testability of systolic arrays with memory in this paper. C-testability implies that the number of test vectors is independent of the size of the array. Integration of test in the design phase of systolic arrays is possible and can be automated with minimal effort. General necessary and sufficient conditions have been derived for classes of iterative arrays by several authors that make them C-testable.

We propose a scheme for C-testing one dimensional sequential arrays. Algorithms to verify the functionality of one dimensional arrays of sequential processors are described. We prove that a constant number of test vectors will suffice to test the entire modified array. Hardware modifications needed to make the sequential array C-testable are described.

The testing time is much shorter in our schemes compared to the conventional LSSD approaches.

14. SUBJECT TERMS
terms

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4. TITLE AND SUBTITLE
VLSI Layout Expectations

5. FUNDING NUMBERS
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6. AUTHORS
C-S Fuh, R.M. Owens, and M.J. Irwin

7. PERFORMING ORGANIZATION NAME AND ADDRESS
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11. SUPPLEMENTARY NOTES
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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12b. DISTRIBUTION CODE

13. ABSTRACT

We are developing a set of CAD tools to assist in the design of certain architectures. This summary describes one of these tools, a VLSI layout assembler called ARTIST. ARTIST performs transistor placement and interconnect. The labeling of ARTIST as a silicon assembler is due to the tightness between the logic description and the layout generated by ARTIST from that description. ARTIST owes its existence to both pragmatic and academic reasons. The academic reason was to provide a test bed so that different approximation algorithms for efficiently finding near optimal layout could be tried. A modular software design was used so that we can easily try different approximation algorithms for transistor placement. The pragmatic reason is that growing need to be able to quickly generate layouts for projects and to be able to quantitatively evaluate many different architecture alternatives. The input supplied to ARTIST is a logic description of a module expressed in a language we call GLUE (Gate LangUagE). The output generated by ARTIST is a VLSI layout of that module in a static CMOS logic gate structure. Novel ideas used in the design of the silicon assemble are described. A comparison between different annealing approaches for transistor placement is presented.

14. SUBJECT TERMS
CAD tools, VLSI layout, silicon assemblers, simulated annealing

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4. TITLE AND SUBTITLE
An Algorithm to Solve IIR Filters by Using DFTs

5. FUNDING NUMBERS
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6. AUTHORS
C-M Wu and R.M. Owens

7. PERFORMING ORGANIZATION NAME AND ADDRESS
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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13. ABSTRACT

This paper proposes a new method to transform an equation of the IIR filter into a form that can be solved by using the discrete Fourier transform (DFT). The algorithm consists of two steps - a DFT step and a correction step - and uses an overlap-save method.

14. SUBJECT TERMS
Digital signal processing, discrete Fourier transforms, IIR filters

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4. TITLE AND SUBTITLE
The Arithmetic Cube

5. FUNDING NUMBERS
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6. AUTHORS
R.M. Owens and M.J. Irwin

7. PERFORMING ORGANIZATION NAME AND ADDRESS
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13. ABSTRACT

We present the design of a VLSI processor which can be programmed to compute the discrete Fourier transform of a sequence of n points and which achieves the theoretical AT^2 lower bound of $\Omega(n^2)$ for $n \in n$ where n is an infinite set. Furthermore, since the set n is also sufficiently dense, the processor achieves for any n the theoretical AT^2 lower bound of $\Omega(n^{2})$ for computing the cyclic convolution of two sequences of n points. Uniquely, our design achieves this bound without the use of data shuffling or long wires. Also, the processor uses only $\sqrt{n}$ multipliers, while many other designs need $\Theta(n)$ multipliers to achieve the same time bounds. Since multipliers are usually much larger than adders, the processor presented in this paper should be smaller. The design also features layout regularity, minimal control, and nearest neighbor interconnect of arithmetic cells of a few different types. These characteristics make it an ideal candidate for VLSI implementation.

14. SUBJECT TERMS
Cyclic convolution, digit signal processing, discrete Fourier transofrm, mixed radix, prime factor, systolic architecture, VLSI architecture

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Multidimensional Algorithms for the Arithmetic Cube

5. FUNDING NUMBERS
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6. AUTHORS
R.M. Owens and M.J. Irwin

7. PERFORMING ORGANIZATION NAME AND ADDRESS
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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13. ABSTRACT

In this paper we consider the problem of computing an arbitrary size discrete Fourier transform or cyclic convolution on a fixed size VLSI processor we call the Arithmetic Cube. We show how either the discrete Fourier transform of n points or the cyclic convolution of two length n sequences can be performed on the Arithmetic Cube whose area is A in time $O(n/\sqrt{A}\log(n/\sqrt{A})+\sqrt{n})$. This bound is within a $\log(n/\sqrt{A})$ factor of the lower bound of $AT^2=\Omega(n^2)$. Note that even if n and A differ by several orders of magnitude, this factor is small. Furthermore, even for a small Arithmetic Cube, our bound is no worse than performing the fast Fourier transform.

14. SUBJECT TERMS
Discrete Fourier transforms, cyclic convolution, VLSI processors

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4. TITLE AND SUBTITLE
A High Level Synthesis Tool for Systolic Designs

5. FUNDING NUMBERS
DAAL03-87-K-0118

6. AUTHORS
P-P Hou, R.M. Owens, and M.J. Irwin

7. PERFORMING ORGANIZATION NAME AND ADDRESS
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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13. ABSTRACT

DECOMPOSER is a high level synthesis tool for automating the design of systolic systems. It is the newest entry in a tool set currently under development at Penn State. DECOMPOSER takes as inputs a hierarchical description of the computation to be performed and some hint as to how it is to be performed. The computation description is in the form of a parametered dag (directed acyclic graph) so that different problem sizes can be handled. The hint is in the form of marking information for that dag. DECOMPOSER produces a detailed report on the hardware requirement for the specified computation. In particular, the structure of each computation node, how the computation nodes are connected, and the input and output sequences are given. This information will be passed to other tools in the tool set so that ultimately a layout description file in suitable format (e.g., CIF) can be generated for the architecture performing the computation derived by DECOMPOSER.

14. SUBJECT TERMS
System synthesis tools, systolic arrays, hierarchical dag computation description

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DECOMPOSER: A Synthesizer for Systolic Systems

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6. AUTHORS
P-P Hou, R.M. Owens, and M.J. Irwin

7. PERFORMING ORGANIZATION NAME AND ADDRESS
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12b. DISTRIBUTION CODE

13. ABSTRACT

A tool for synthesizing systolic systems is introduced. Given a hierarchical specification of the computations to be performed and hints as to how these computations are to be performed, this tool generates an analysis of the hardware required to do the computations. The computations are specified as directed acyclic graphs and the hints tell the temporal and topological relationships of each computation. The systolic system is synthesized by traversing the graph and marking each computation with a processor name and a time stamp. This tool, called DECOMPOSER, is the newest entry in a tool set currently under development at Penn State. Its output can subsequently be fed to the remaining tools in the tool set to generate a VLSI fabrication description of the systolic system.

14. SUBJECT TERMS
System synthesis tools, systolic arrays, hierarchical dag computation description

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4. TITLE AND SUBTITLE
A Comparison of Two Digit Serial VLSI Adders

5. FUNDING NUMBERS
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6. AUTHORS
M.J. Irwin and R.M. Owens

7. PERFORMING ORGANIZATION NAME AND ADDRESS
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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12b. DISTRIBUTION CODE

13. ABSTRACT

The VLSI design of two digit serial adders, one which processes operand digits and produces on-line result digits least significant digit first and one which processes operand and produces on-line result digits most significant digit first, is presented. They are compared with respect to number of gates, interconnect lines, layout area, and digit and operand add time. An optimal gate level description for one of the adders is given. This gate level description can be input to a layout tool to automatically produce the CMOS gate matrix layout of the description. Finally, word parallel adders built out of the two digit serial adders are discussed and compared.

14. SUBJECT TERMS
Digit serial addition, digit on-line processing, least and most significant digit first addition

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4. TITLE AND SUBTITLE
A VLSI Space Warper

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6. AUTHORS
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7. PERFORMING ORGANIZATION NAME AND ADDRESS
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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12b. DISTRIBUTION CODE

13. ABSTRACT

In this paper we consider the problem of building a VLSI processor array which can be used to determine how well two two-dimensional images match. Such an array can be used to form the basis of an image recognition system. The design is based on being able to expand and contract the two images with respect to one another so that a best matching is obtained. In this way, the Space Warp VLSI array is the two-dimensional analog to the Time Warp array for one dimensional signals typically used in isolated word recognition. We show that an efficient and robust VLSI design is possible if local feature matching is used.

14. SUBJECT TERMS
Two-dimensional pattern matching, VLSI processor arrays, time and space warping, local feature matching

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4. TITLE AND SUBTITLE
A VLSI Design System for Signal Processors

5. FUNDING NUMBERS
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6. AUTHORS
M.J. Irwin and R.M. Owens

7. PERFORMING ORGANIZATION NAME AND ADDRESS
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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12b. DISTRIBUTION CODE

13. ABSTRACT

This paper overviews a set of CAD tools under development to support the rapid prototyping of a family of VLSI signal processing architectures. The feasibility of a wide variety of such architectures could then be quickly evaluated at the layout level using the tool set. Our class of architectures is first introduced. Properties that make them unique, amenable to VLSI, and high performance are discussed. Then, a set of tools to support the rapid prototyping of those architectures is presented. A section is devoted to each of the steps in the design process - system synthesis, module synthesis, module generation, system generation, and finally system validation. Ultimately, user supplied input to the CAD system will be a high-level, algorithmic description of the signal processing application. The output of the CAD system will be the layouts for the chip set of the architecture which solves that application.

14. SUBJECT TERMS
CAD tools, VLSI signal processing architectures, synthesis, generation, and validation tools

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6. AUTHORS
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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12b. DISTRIBUTION CODE

13. ABSTRACT

This paper will present a CAD tool set designed for rapid prototyping a specific class of high performance signal processing architectures. Efficient implementation of these architectures results in systems that are very fast (< 35 nsec clock cycle) and which can be very small in size (< 500 λ by 500 λ). Our CAD system is composed of five software tools which have been designed to work together. The designer inputs an algorithmic description of the application architecture as input and the design system outputs the layouts of the chip set for the application architecture. While many of these tools require a large amount of run time, they allow the efficient automatic production of chip sets for applications which before could only be done by hand and therefore were virtually intractable problems.

14. SUBJECT TERMS
CAD tools, VLSI signal processing architectures, VLSI design process

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4. TITLE AND SUBTITLE
Design Issues in Digit Serial Signal Processors

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6. AUTHORS
M.J. Irwin and R.M. Owens

7. PERFORMING ORGANIZATION NAME AND ADDRESS
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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13. ABSTRACT

This paper presents several design issues which have arisen during the development of a set of CAD tools used to support the rapid prototyping of a family of VLSI signal processing architectures. The components out of which our signal processors are constructed are ones which operate digit serially. Digit serial architectures, which have digit serial data transmission combined with digit serial computation, are uniquely suited for the design of VLSI signal processors. The speed disadvantages of digit serial input are overcome if the input is overlapped with the computation - what we refer to as digit pipelining. Thus, digit serial architectures can provide both high throughput and low latency. Design tradeoffs affecting the component design as well as the system design for digit serial signal processors are presented. Considerations which have affected the development of our CAD tools will be discussed.

14. SUBJECT TERMS
Digit serial components, digit pipelining, signal processing, design tradeoffs

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4. TITLE AND SUBTITLE
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6. AUTHORS
R.M. Owens and M.J. Irwin

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12b. DISTRIBUTION CODE

13. ABSTRACT

We consider in this paper the problem of developing VLSI signal processors for computing convolutions. Convolutions can be efficiently computed by VLSI processors which consist of arrays of adders when stated in the following form

$$y = C(B\,h \circledast A\,x) \quad .$$

where the elements of **C**, **B**, and **A** consist of only 1, 0, or −1. Unfortunately, when stated in matrix form the published algorithms have matrices with elements other than 1, 0, or −1. We first explore why this occurs. We then show how it may be prevented when an algorithm is developed. Failing that, we propose a technique for addressing this problem which consists of replacing each such matrix by the product of two or more matrices whose elements are 1, 0, or −1.

14. SUBJECT TERMS
Fast convolution algorithms, discrete Fourier transforms, polynomial multiplication, adder arrays

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4. TITLE AND SUBTITLE
Digit Serial Systolic VLSI Architectures

5. FUNDING NUMBERS
DAAL03-87-K-0118

6. AUTHORS
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7. PERFORMING ORGANIZATION NAME AND ADDRESS
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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13. ABSTRACT

Digit serial systolic architectures, which have digit serial data transmission combined with digit serial computation, are uniquely suited for the VLSI implementation of many special-purpose processors. In signal processing applications where communication issues dominate and high speed is important, they are particularly appropriate. The speed disadvantages of digit serial input are overcome if the input is overlapped with the computation - what we refer to as digit pipelining. Digit pipelining allows us to break up long strings of combinatorial logic and, thus, to increase the clock rate of the system while still preserving much of the circuit structure. In general, for a modest increase in hardware (with in VLSI translates to a modest increase in area) digit serial architectures offer the potential of higher throughput than equivalent word parallel architectures. Designs for various digit serial adders are detailed. Two systolic filter architectures are then presented which use the digit serial adders.

14. SUBJECT TERMS
Digit serial systolic architectures, digit pipelining, signal processing, systolic filters

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4. TITLE AND SUBTITLE
Using VHDL as a Language for Synthesis of CMOS VLSI Circuits

5. FUNDING NUMBERS
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6. AUTHORS
S. Levitan, A. Martello, R.M. Owens, and M.J. Irwin

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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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12b. DISTRIBUTION CODE

13. ABSTRACT

The Very High Speed Integrated Circuits (VHSIC) Hardware Description Language (VHDL) was designed primarily for documentation and modeling of complex digital systems. We have used this language as a design description language for our VLSI synthesis system and have successfully generated mask geometries for several complex designs. We have found that some of the VHDL data-flow and structure building constructs are very appropriate for describing VLSI designs, while other constructs have little or no meaning in a synthesis environment. We have defined a set of synthesis semantics for a restricted set of structural and behavioral constructs of the VHDL language. We examine some of these issues and report on our work on synthesis of layout from VHDL structural and behavioral models.

14. SUBJECT TERMS
VHDL (VHSIC Hardware Description Language), synthesis, CAD tools, VLSI design process

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4. TITLE AND SUBTITLE
A Comparison of Four Two-Dimensional Gate Matrix Layout Tools

5. FUNDING NUMBERS
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6. AUTHORS
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13. ABSTRACT

A comparison of four layout tools is presented. The layout style is a two-dimensional gate matrix. The first layout tool discussed uses "standard" simulated annealing. Annealing on gate clusters instead of individual gates can be used to improve the layout results. Two different ways of determining good gate clusters for use in the annealing process are compared. The first way uses clusters derived from user specified gate hierarchies, while the second determines clusters based on gate connectivity. The fourth layout tool uses a decomposition scheme based on quadrisection. Layout results for a set of benchmark circuits are presented for each of the tools.

14. SUBJECT TERMS
CAD tools, gate matrix layout, simulated annealing, clustering, quadrisection

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4. TITLE AND SUBTITLE
Multi-Level Logic Synthesis Using Communication Complexity

5. FUNDING NUMBERS
DAAL03-87-K-0118

6. AUTHORS
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13. ABSTRACT

We present a new multi-level logic synthesis technique based on minimizing communication complexity. Intuitively, we believe this approach is viable because for many types of circuits lower bounds on the area needed to implement those circuits have been obtained considering only communication complexity. It performs especially well for functions which are hierarchically decomposable (e.g., adders, parity generators, comparators, etc.). Unlike many other multi-level logic synthesis techniques, a lower bound can be computed to determine how well the synthesis was performed. We also present a new multi-level logic synthesis program based on the techniques described for reducing communication complexity.

14. SUBJECT TERMS
CAD tools, multi-level logic synthesis, communication complexity, partitioning, balanced and unbalanced decompositions

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Distributed Fault Diagnosis in the Butterfly Parallel Processor

5. FUNDING NUMBERS
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6. AUTHORS
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13. ABSTRACT

This paper is concerned with a distributed, system level fault diagnosis in the BBN Butterfly Parallel Processor employing a multistage network with 4 x 4 switching elements. Several previous works in distributed diagnosis focus on the interconnection network itself, so that they can assume the processor nodes are fault free to interpret the diagnostic information. However, to be more realistic for an entire multiprocessor diagnosis, the effect of a single fault should be able to affect the integrity of computation results, or misdirect the messages transferred, or corrupt the data transmitted. Our proposed approach attempts to detect and locate single faults caused by processor nodes or switching elements or communication links. The diagnosis of a limited number of multiple faults is also discussed.

14. SUBJECT TERMS
Fault diagnosis, multistage interconnection networks, butterfly parallel processor

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Parallel Algorithms for Region Labeling on a Memory Array Architecture

5. FUNDING NUMBERS
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6. AUTHORS
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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12b. DISTRIBUTION CODE

13. ABSTRACT

In this paper we propose a parallel algorithm for region (connected component) labeling on a simple memory array architecture we call the *Access Constrained Memory Array Architecture* (ACMAA). The ACMAA consists of a linear array of processors concurrently accessing row or columns of an array of memory modules. This organization has a simple and regular structure and hence is very efficient for VLSI implementation. Our region labeling algorithm is based on a bottom-up, divide-and-conquer strategy. We describe an algorithm for an image of size N x N on an ACMAA of size N with a running time complexity of $O(N^2)$. The algorithm can also be easily generalized to take care of larger size images by storing subimages instead of just one pixel in each memory module.

14. SUBJECT TERMS
Machine vision, VLSI architectures, region labeling

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4. TITLE AND SUBTITLE
The Arithmetic Cube: A Highly Parallel VLSI DSP Architecture

5. FUNDING NUMBERS
DAAL03-87-K-0118

6. AUTHORS
R.M. Owens, M.J. Irwin, T. Kelliher, and C-M Wu

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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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13. ABSTRACT

Experience gained in building a VLSI processor for computing the cyclic convolution and DFT are discussed. The processor, which we call the Arithmetic Cube, is designed to solve small-n algorithms. Intuitively, the architecture for the small-n algorithms is an array of *nxnxp* cells, where *p* is the precision of the numbers. Using digit-pipelined techniques, we can reduce this architecture to either a *nxn* or a *nxp* adder array. The first generation Arithmetic Cube was based on the *nxn* array. We explain how the first Arithmetic Cube could compute DFTs using an *nxn* array. Experiences learned from this design are discussed. Building on this experience, a second generation Arithmetic Cube based on the *nxp* array has been defined. Plans for building the second generation Cube, including documentation and simulation using VHDL, are presented.

14. SUBJECT TERMS
Discrete Fourier transforms, cyclic convolution, VLSI processor, adder arrays

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4. TITLE AND SUBTITLE
Chinese Character Recognition Based on a New Template Matching Algorithm

5. FUNDING NUMBERS
DAAL03-87-K-0118

6. AUTHORS
C-M Wu, R.M. Owens, and M.J. Irwin

7. PERFORMING ORGANIZATION NAME AND ADDRESS
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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12b. DISTRIBUTION CODE

13. ABSTRACT

A new template matching algorithm is used for the recognition of Chinese characters. This new algorithm combines feature, flexible, and structural matchings. First, for feature matching, any local feature can be used. Local features include junctions, end points, line points, directions, curvatures, and boundaries. Second, for flexible matching, the concept of space warping is used. This means that each point of the reference template can match a range of points of the input template. Third, for structural matching, structural information is used implicitly and dynamic programming is used to accumulate the local distances into a global distance. Thus, the orderings in the reference templates are preserved well. Using eighteen groups of Chinese characters, we show that this new algorithm can solve some of the difficulties met by Japanese researchers using only 0/1 images. We also show that this new algorithm can greatly improve the performance of the traditional template matching algorithm (correlation).

14. SUBJECT TERMS
Character recognition, template matching, local features, space warping, dynamic programming

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4. TITLE AND SUBTITLE
An Efficient Implementation of Message Combining

5. FUNDING NUMBERS
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6. AUTHORS
P-P Hou, M.J. Irwin and R.M. Owens

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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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13. ABSTRACT

In MIMD shared memory parallel computers "combining" is used to reduce memory contention which generally occurs for shared lock and synchronization variables. This problem if unresolved, leads to the tree saturation effect and severely degrades the performance of the machine. While several projects already incorporate this technique into their designs, they use two-way combining; i.e., memory requests for the same address are combined pair-wise. Two-way combining was shown to be unable to eliminate tree saturation. Three-way and unbound combining is adequate for solving this problem but whether it can be efficiently implemented was unknown. This paper presents an efficient implementation of unbounded combining using a content addressable memory.

14. SUBJECT TERMS
MIMD shared memory computers, combining, tree saturation, content addressable memory

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4. TITLE AND SUBTITLE
Distance Measuring Problems in Image Recognition Systems

5. FUNDING NUMBERS
DAAL03-87-K-0118

6. AUTHORS
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7. PERFORMING ORGANIZATION NAME AND ADDRESS
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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12b. DISTRIBUTION CODE

13. ABSTRACT

This paper presents a new image matching algorithm; we call this algorithm the dynamic space warping algorithm (DSWA). The algorithm consists of two parts: a distance measuring scheme and a dynamic programming algorithm. DSWA can solve space warping problems (e.g., shrinking, enlarging, rotation, and distortion) with good performance by embedding controllable flexibility (or warping). The concept of flexibility can be explained by using local-distance diagrams. With flexibility, the local-distance diagram between two two-dimensional images is four-dimensional and is generated using a certain distance measuring scheme. Based on compression and expansion, the dynamic programming algorithm of the DSWA computes a minimum distance from the four-dimensional local-distance diagram. Experimental results have shown that the recognition performance will be affected greatly by the distance measuring scheme used. Thus, after briefly presenting the DSWA, we will focus on the topics related to local-distance measuring. These topics include don't care regions, don't care points, feature relaxations, and multistage template matching.

14. SUBJECT TERMS
Image recognition, dynamic space warping, local-distance diagrams, dynamic programming, feature relaxation, multistage template matching

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6. AUTHORS
M.J. Irwin and R.M. Owens

7. PERFORMING ORGANIZATION NAME AND ADDRESS
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13. ABSTRACT

Digit serial architectures, which have digit serial data transmission combined with digit serial computation, are uniquely suited for the design of VLSI signal processors. The speed disadvantages of digit serial input are overcome if the input is overlapped with the computation - what we refer to as digit pipelining. Digit pipelining allows us to break up long strings of combinatorial logic and, thus, to increase the clock rate of the system while still preserving much of the circuit structure. In general, for a modest increase in hardware (which in VLSI translates to a modest increase in area) digit serial architectures offer the potential of higher throughput than equivalent word parallel architectures. Several designs for various digit serial adders are presented. Then two filter examples are discussed which use the digit serial adders to achieve digit pipelining.

14. SUBJECT TERMS
Digit serial processing, digit pipelining, most significant first processing, FIR filters, IIR filters, VLSI implementation

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5. FUNDING NUMBERS
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6. AUTHORS
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7. PERFORMING ORGANIZATION NAME AND ADDRESS
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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13. ABSTRACT

In this paper we consider a new, very fine-grained architecture which can solve certain two-dimensional machine vision problems very efficiently. The architecture we present maintains both a high degree of flexibility and fine-grainness. This is done by reducing each processor to an associative memory cell. However, unlike classical associative memory processors, our processor uses a two-dimensional nearest-neighbor interconnect. Arithmetic operations are based on the use of a redundant number sytstem and a physically compact memory word structure. These features provide a high level of performance.

14. SUBJECT TERMS
Associative processing, two-dimensional interconnect, redundant number representation, two-dimensional Laplacian, connected component labeling

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Distortion Processing in Image Matching Problems

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6. AUTHORS
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13. ABSTRACT

In this paper we present a new image matching algorithm, which we call the dynamic space-warping algorithms (DSWA), that is based on both local-distance diagrams and dynamic programming. DSWA can solve space warping problems (e.g., shrinking, enlarging, rotation, and distortion) with good performance by embedding controllable flexibility (or warping). The concept of flexibility can be explained well using local-distance diagrams. With flexibility, the local-distance diagram between two two-dimensional images is four dimensional. Based on compression and expansion, DSWA generates a minimum distance from the four-dimensional local-distance diagram. Experimental results have shown that DSWA is very reliable.

14. SUBJECT TERMS
Image recognition, dynamic space-warping algorithms, local-distance diagrams, shrinking enlarging, rotation, distortion

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Being Stingy with Multipliers

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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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13. ABSTRACT

It is the thesis of this paper that from an implementation point of view it is often the case that the chip area occupied by a VLSI signal processor is dominated and, therefore, largely determined by the area which must be devoted to multipliers. Therefore, signal processors which have high multiplier utilization (i.e., attain a high throughput for a given number of multipliers) are of interest because it is possible for them to also attain good VLSI area utilization. We present several signal processing architectures which have optimal multiplier utilization. We compare these architectures to several more conventional alternatives. We also demonstrate how our architectures achieve better multiplier utilization and, hence, VLSI are utilization without suffering a degradation in utilization of other resources (e.g., adders and interconnect).

14. SUBJECT TERMS
Digital signal processing, VLSI, convolution, area efficient transforms, digit pipelining, problem pipelining

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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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13. ABSTRACT

In this paper we explain how we applied a design methodology to the design of a Winograd FFT processor. Through this design process, we have learned that a good simulation language (such as VHDL) can make the design cycle faster and more reliable. Eventually, the design system based on VHDL should combine simulation, synthesis, and testing. Such a design system will be very suitable fore designing algorithm oriented VLSI systems.

14. SUBJECT TERMS
Simulation, synthesis, test, VHDL, Winograd FFT processor

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4. TITLE AND SUBTITLE
Mapping High-Dimension Wavefront Computations to Silicon

5. FUNDING NUMBERS
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6. AUTHORS
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13. ABSTRACT

In this paper we present a new template matching algorithm with good recognition performance. However, this new algorithm exhibits a complex, four-dimensional, wavefront architecture. Thus, for VLSI implementation, reduced architectures with fewer connections and processors need to be derived. For this purpose, we develop a systematic reduction methodology to manually map wavefront computations from high dimensions to low dimensions. (This methodology consists of seven steps.) Finally, based on this seven step reduction methodology, we derive several two-dimensional architectures (which are suitable for VLSI implementation) for the new template matching algorithms and have simulated one of them.

14. SUBJECT TERMS
Template matching, wavefront architectures. VLSI, data dependency graphs, dynamic warping algorithms

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Test Generation in Circuits Constructed by Input Decomposition

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6. AUTHORS
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13. ABSTRACT

The logic synthesis tool FACTOR developed at Penn State generated circuits by finding the best decomposition of the inputs to minimize the communication complexity. It tries to minimize the number of connections in the circuit, instead of the number of gates, for area optimization. In addition tot eh area optimization, FACTOR also has the nice feature of generating circuits for which test vectors can be easily generated. Because it tries to find an input partitioning which provides the minimal number of connections between subcircuits, the generated circuits are tree type with restricted reconvergent fanouts. In these restricted tree type circuits, the test generation problem can be solved in *polynomial time* with certain constraints which are usually satisfied by FACTOR generated circuits. In this case, the problem of test generation can be solved simultaneously with the area optimization problems. In this paper, we show how improved testability can be achieved at the same time as area optimization by presenting an efficient test generation algorithm for the restricted tree type circuits generated by FACTOR using single stuck type fault model.

14. SUBJECT TERMS
communication complexity based logic synthesis, test generation, restricted reconvergent fanout circuits, stuck at fault model

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T-T Hwang, R.M. Owens and M.J. Irwin

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13. ABSTRACT

In this paper we consider the problem of configuring a programmable logic device (PLD) wo that some given function is computed by the device. Obtaining the information necessary to configure a PLD entails both logic synthesis and logic embedding. Due to the very constrained nature of the embedding process, this problem differs from traditional multilevel logic synthesis in that the structure (or lack thereof) of the synthesized logic is much more important. Furthermore, a metric like literal count is much less important. We present a method which appears to be more suited to this problem than other multilevel logic synthesis methods.

14. SUBJECT TERMS
programmable logic devices, multilevel logic synthesis, logic embedding, communication complexity based logic synthesis

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6. AUTHORS
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13. ABSTRACT
We present in this paper a multi-level logic synthesis technique based on minimizing communication complexity. Intuitively, we believe this approach is viable because for many types of circuits lower bounds on the area needed to implement those circuits have been obtained considering only communication complexity. This approach performs especially well for function which are hierarchically decomposable (e.g., adders, parity generators, comparators, etc.). Unlike many other multi-level logic synthesis techniques, a lower bound can be computed to determine how well the synthesis was performed. We also present a new multi-level logic synthesis program based on the techniques described for reducing communication complexity.

14. SUBJECT TERMS
CAD tools, multi-level logic synthesis, communication complexity, partitioning, balanced and unbalanced decompositions

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The Design of the Arithmetic Cube II

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6. AUTHORS
T. Kelliher, C-M Wu, R.M. Owens and M.J. Irwin

7. PERFORMING ORGANIZATION NAME AND ADDRESS
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13. ABSTRACT

The Arithmetic Cube is a high performance signal processing architecture which implements the so-called small n algorithms for solving DFT and CC problems. We have built one version of the Cube, learning much from the impact which our architectural decisions made upon the implemented Cube. Currently, we are buidling a second version of the Cube. Extensive VHDL simulation has played an important role in shaping the final design. We discuss the two sets of lessons learned from the first Cube and from the simulation of the second Cube.

14. SUBJECT TERMS
architecture design, small n algorithms, discrete Fourier transforms, cyclic convolutions, VHDL simulation

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A Digit Pipelined Dynamic Time Warp Processor

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6. AUTHORS
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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13. ABSTRACT

A custom CMOS systolic design is presented which can achieve real-time isolated word recognition for large dictionaries. The design is based on the dynamic time warping (DTW) algorithm, an exhaustive search technique which permits nonlinear pattern matching between an unknown utterance and a reference word. Our design differs from previous systolic DTW designs in that (1) all data is represented in signed-digit, base 4 format; (2) digits are passed between processing elements in a most significant digit first, digit serial fashion; and (3) the algorithms are pipelined at the digit level. Using most significant digit first data flow allows digit pipelining to succeed where conventional bit-serial pipelining has failed for the arithmetic operations required in the DTW algorithm. This allows a very high degree of concurrency and a high data rate to be maintained, while the pin out requirements are kept low. As many as twenty-five DTW processing elements will fit on one 128 pin chip. The VLSI DTW design presented is both flexible and modular. It is independent of the number of coefficients per frame and their precision. The design is also easily expandable in the number of frames per word and the warp factor used to achieve the nonlinear matching.

14. SUBJECT TERMS
Isolated word recognition, dynamic time warping, systolic meshes, digit pipelining, signed-digit representation, most significant digit first processing

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Digit Serial Multipliers

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6. AUTHORS
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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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13. ABSTRACT

Digit serial data transmission can be used to an advantage in the design of special purpose processors where communication issues dominate and where digit pipelining can be used to maintain high data rates. VLSI signal processing is one such problem domain. We propose detailed designs of unidirectional systolic and semi-systolic programmable digit pipelined (serial) multipliers. These multipliers are programmable; i.e., one operand is pre-stored in the multiplier and the other operand is fed in a digit serial fashion. The VLSI implementation of the systolic multiplier is given. This systolic multiplier is used in our VLSI signal processing system. Lastly, for the sake of completeness we also propose designs of nonprogrammable unidirectional and bidirectional digit serial multipliers.

14. SUBJECT TERMS
Digit serial data transmission, digit pipelining, systolic and semi-systolic linear arrays, digit pipelined multipliers

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6. AUTHORS
T. Kelliher, K-K Leung, R.M. Owens and M.J. Irwin

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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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13. ABSTRACT
In this paper we describe the synthesis, design and simulation of the Arithmetic Cube II, a second generation, high performance digital signal processing architecture. The architecture implements the so-called small *n* algorithms. We are currently building a prototype system which should be capable of computing a 1024 point complex DFT in 410 microseconds.

14. SUBJECT TERMS
digital signal processing, small *n* algorithms, discrete Fourier transforms

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Image Processing on a VLSI-Based Memory Array Architecture

5. FUNDING NUMBERS
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6. AUTHORS
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13. ABSTRACT

In this paper we examine the usefulness of a simple memory array architecture to several image processing tasks. This architecture, called the *Access Constrained Memory Array Architecture* (ACMAA) has a linear array of processors which concurrently access distinct rows or columns of an array of memory modules. ACMAA is efficient for VLSI implementation because of its modular structure, simple interconnect, and limited global control. Its row and column bus structure provide it with efficient local as well as global communication capabilities. This property of ACMAA makes it very suitable for solving problems in image processing and computer vision. All the ACMAA algorithms presented in this paper achieve a linear speed-up over the corresponding fast sequential algorithms.

14. SUBJECT TERMS
Image processing and computer vision, VLSI architectures, discrete Fourier transform, convolution, image histogramming, contrast enhancement, edge detection

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12a. DISTRIBUTION/AVAILABILITY STATEMENT
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13. ABSTRACT

In this paper we consider using "digit serial" processing to build high performance parallel structures, in particular parallel signal processors. Digit serial arithmetic processors have digit serial data transmission combined with digit serial computation. Three digit serial arithmetic processors are presented and compared with their digit parallel counterparts. We show that by using a digit serial approach we can achieve a higher throughput than with a digit parallel processor, even though the two processors are structurally similar and have components of similar complexity.

14. SUBJECT TERMS
digit serial processing, digit parallel processing, digit serial arithmetic, signal processors

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6. AUTHORS
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13. ABSTRACT

This paper examines the error performance and presents simulation results of the Arithmetic Cube. The Arithmetic Cube is a special purpose architecture for computing high speed convolution and the DFT. An error analysis of convolution and the DFT, as computed on the Cube, is done. An upper bound on the number of bits lost is derived. The Cube loses at most an extra two bits (four bits), while computing convolution (DFT), more than the number of bits lost if computed by the direct, limited precision convolution (DFT). A VHDL description of the Cube was written and simulations were run. Simulation results substantiate the derived upper bounds. A comparison of the Winograd Fourier Transform Algorithm (WFTA), computed by the Cube, and a rounded FFT, shows that the Cube is at least as accurate as the rounded FFT. Contrary to previous results, it is argued that the WFTA performs better, with respect to accuracy, than the Prime Factor Algorithm (PFA), if both are computed on the Cube.

14. SUBJECT TERMS
error analysis, accuracy, convolution, discrete Fourier transform, Winograd Fourier transform

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13. ABSTRACT

In this paper we present a new, very fine grain architecture. Very fine grain architectures are especially suited for problems with a high degree of parallelism. However, to maintain their fine graininess most fine grain processors are relatively inflexible. Any attempt to increase flexibility increases processor complexity and, thereby, decreases grainness. The architecture we present in this paper maintains both a high degree of flexibility and fine grainness. This is done by reducing each processor to an associative memory cell. However, unlike other associative memory processors, ours uses a two-dimensional interconnect and a physically compact memory word structure. Arithmetic operations are based on the use of redundant number system. These features provide an even higher level of performance. This is particularly true for certain two-dimensional problems which we show can be solved very efficiently on our architecture.

14. SUBJECT TERMS
Associative processing, fine grain architectures, two-dimensional interconnect, redundant number representation, two-dimensional Laplacian, sorting, FFT

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13. ABSTRACT

In this paper, we present a new addition algorithm - ELM. This algorithm makes use of a tree of simple processors and requires o($log\ n$) time, where n is the number of bits in the augend and addend. The sum itself is computed in one pass through the tree. This algorithm was discovered by a VLSI CAD tool, FACTOR, developed at Penn State for use in synthesizing CMOS VLSI circuits.

14. SUBJECT TERMS
Addition, carry look-ahead addition, fast addition, logic synthesis, tree of processors

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